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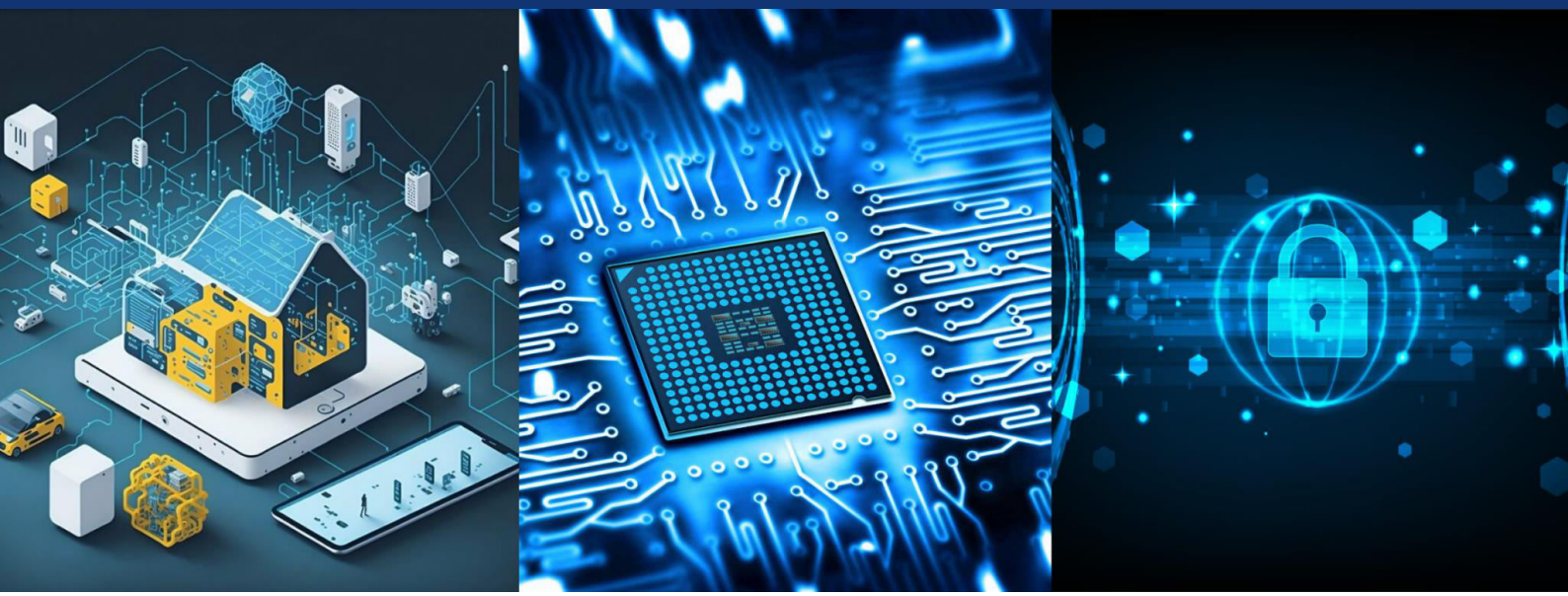

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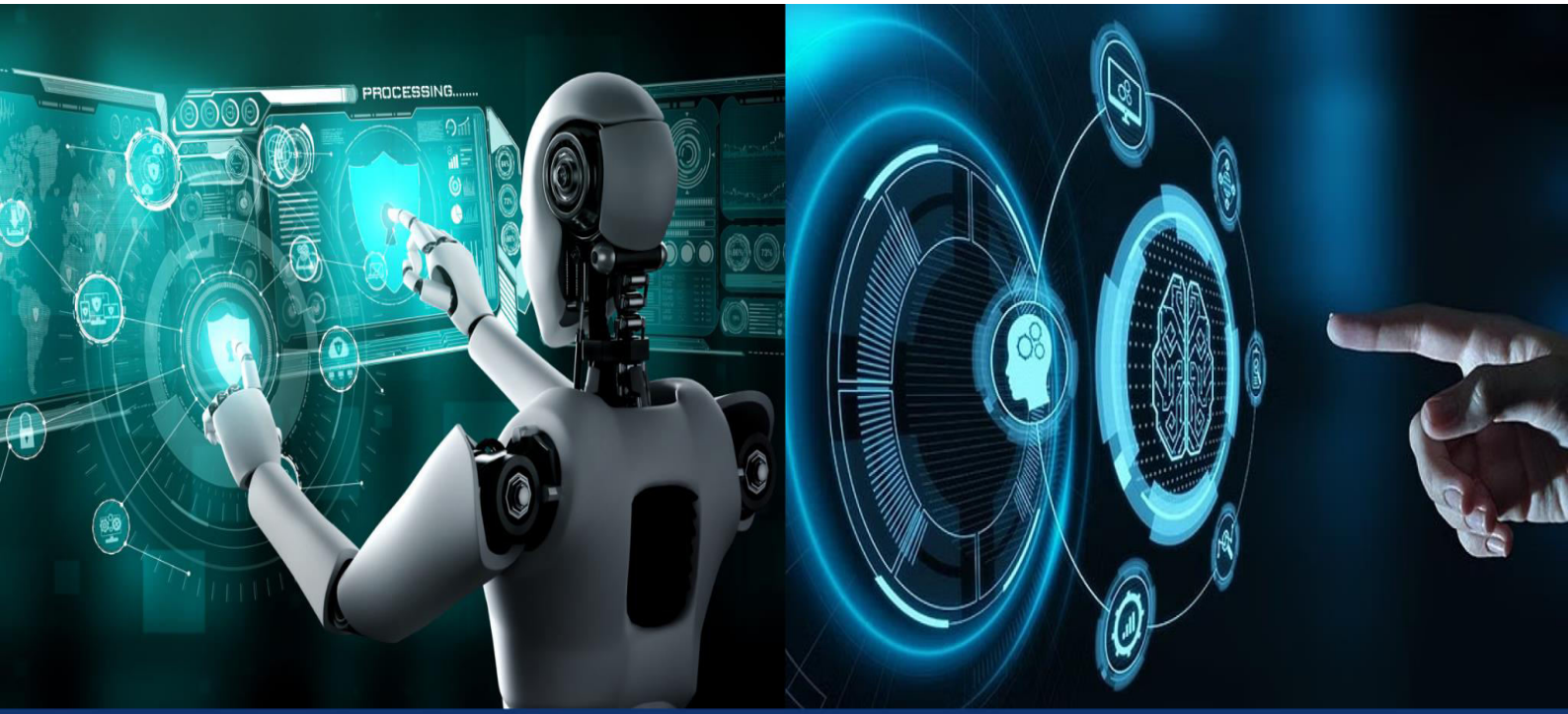

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Performance Analysis of NMOS Power-Gated Approximate Multiplier

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ABSTRACT: This paper describes the design of an approximate multiplier that uses NMOS-based power gating to achieve low power and high-performance operation. The proposed approach integrates NMOS sleep transistors into XOR gate structures to minimize leakage power and reduce unnecessary switching activity during idle conditions. Approximation is mainly applied to the lower significant bits (LSBs), while the higher significant bits (MSBs) are maintained to ensure reliable output behaviour. This method lowers circuit complexity and enhances speed while keeping the critical portion of the result unaffected. The design is implemented using the Tanner EDA tool with 90 nm technology, and its performance is analysed in terms of power consumption, delay, and Power Delay Product (PDP). The results show that the proposed multiplier successfully reduces both dynamic and static power, making it suitable for low-power VLSI applications.

I. INTRODUCTION

In recent years, applications such as image processing, video streaming, and artificial intelligence (AI) have experienced rapid growth. These applications demand high-speed and energy-efficient hardware to process large volumes of data. Among the various operations involved, multiplication plays a crucial role, particularly in neural networks where repetitive computations are performed.

Traditional exact multipliers provide precise results; however, they suffer from high power consumption, increased delay, and larger hardware area. These drawbacks make them less suitable for modern systems such as mobile devices, IoT applications, and embedded platforms, where power efficiency and compact design are essential.

To address these limitations, approximate computing has become an effective approach. It allows a slight and controlled loss in accuracy to achieve better speed, lower power consumption, and improved hardware efficiency. Since many modern applications, especially in the domain of artificial intelligence, can tolerate minor computational errors, approximate multipliers are highly effective in such scenarios.

In this work, an approximate multiplier is designed by simplifying key components such as full adders, half adders, and 4:2 compressors. These components are optimized to reduce computational complexity while maintaining acceptable accuracy. Additionally, NMOS-based power gating is incorporated to minimize leakage power by disabling inactive portions of the circuit. The proposed design is implemented and analyzed using Tanner EDA tools, including S-Edit for schematic design, T-Spice for simulation, and W-Edit for waveform analysis. The main objective is to design a multiplier that maintains a good balance between accuracy, power consumption, and performance, making it suitable for modern low-power applications.

II. RELATED WORK

Approximate multipliers have gained attention in recent years because they improve energy efficiency and speed while keeping acceptable accuracy. Many research works focus on different design methods to achieve a balance between performance and computational precision.

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Fang-Yigu, Ing-Chaolin, and Jia-Wei Lin (2022) proposed a low-power, high-accuracy approximate multiplier using a reconfigurable truncation approach. Their design allows dynamic control of truncation levels, helping adjust accuracy based on application needs. By removing less significant bits and optimizing partial product generation, it reduces power and delay while maintaining good output quality.

Faranaz Sabetzadeh and Mohammad Hossein Moaiyeri (2023) introduced an ultra-efficient approximate multiplier with an error compensation mechanism.The design simplifies partial product computations to reduce hardware complexity, while an additional correction unit minimizes the resulting errors. This approach improves overall accuracy without significantly increasing power or area, making it suitable for error-tolerant applications.

Ayushi Vinodia (2024) developed an energy-efficient approximate multiplier with flexible precision control. The proposed design allows adjustment of approximation levels depending on the required accuracy, enabling a balance between performance and energy consumption. The use of scalable approximation techniques helps reduce power consumption, minimize area, and increase processing speed, making them suitable for applications like multimedia and machine learning.

Zendegani et al. (2017) presented the RoBa (Rounding-Based) multiplier, which utilizes rounding techniques during partial product generation to reduce computational complexity. By approximating less significant operations, the design achieves high-speed performance and significant energy savings. This method demonstrated improvements in delay, power consumption, and area, particularly for digital signal processing applications.

Momeni et al. (2015) conducted a comprehensive study on approximate compressor design for multipliers. Their work introduced efficient 4:2 compressor architectures that reduce hardware requirements while maintaining acceptable accuracy. The study also analyzed the trade-offs between power, area, and error, providing a strong foundation for designing approximate arithmetic circuits.

Yang et al. (2015) further investigated approximate compressors for error-resilient multiplier designs. Their research focused on analyzing how approximation errors propagate through the multiplier structure and proposed design strategies to minimize critical errors while maximizing efficiency. This work contributed to improving the reliability of approximate multipliers.

Lin and Lin (2013) addressed the accuracy limitations of approximate multipliers by incorporating error correction techniques. Their hybrid design combines approximate computation with selective correction mechanisms to enhance output precision. This approach maintains a balance between accuracy and efficiency, making it suitable for applications that require moderate precision.

Overall, these studies highlight various approaches such as truncation, rounding, approximation, and error compensation to design efficient multipliers. However, achieving an optimal balance between power, delay, and accuracy remains a key challenge, motivating further research in this area.

III. EXISTING METHOD

8-Bit Approximate Multiplier Without Power Gating:

Existing approximate multiplier designs aim to improve power efficiency and speed by lowering computational complexity while still maintaining acceptable accuracy. A commonly used approach is to combine approximate arithmetic units, such as 4:2 compressors, with conventional components like full adders and half adders to perform multiplication.

In most traditional designs, approximate multipliers simplify the partial product generation and reduction stages by truncating less significant bits or modifying compressor structures.These methods reduce power consumption, delay, and hardware area. However, such designs often suffer from two major limitations. First, many multipliers provide a fixed trade-off between accuracy and performance, which is determined during the design stage and cannot be changed later. Second, some designs introduce reconfigurability to adjust accuracy, but this typically increases hardware complexity and area overhead.

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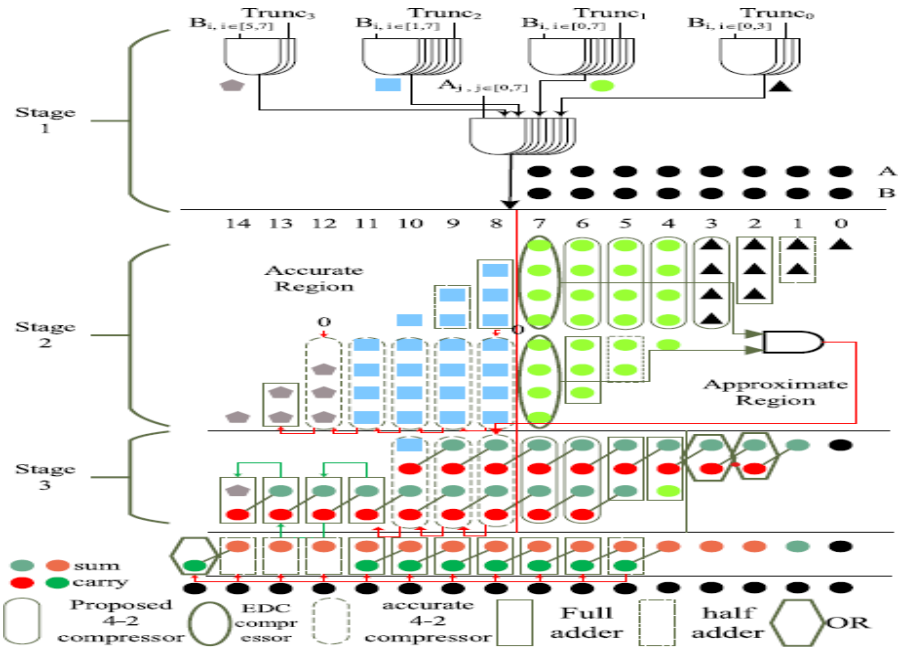
A key component in these multipliers is the 4:2 compressor, which is commonly used to reduce partial products. In conventional accurate designs, 4:2 compressors rely on full adders and include carry propagation between stages, leading to higher delay and power consumption.To address this, approximate compressors simplify the design by reducing inputs, removing carry dependencies, or modifying logic operations. This decreases complexity and increases speed, but it can introduce some errors in the output.

Most existing approximate compressor designs aim to balance accuracy and efficiency by optimizing logic operations and selectively approximating less significant bits. However, errors generated in these compressors can propagate through the multiplier, affecting the final result. Some designs attempt to address this issue by using error compensation or correction techniques, but these methods may increase circuit complexity.

Fig.1. 8 Bit Approximate Multiplier



The figure shows the structure of partial product generation and accumulation in an 8-bit approximate multiplier,where the dot diagram representation depicts the systematic arrangement of partial products produced during the multiplication of two 8-bit input operands, with each dot corresponding to a single bit position in the partial product array. The upper triangular portion of the diagram represents the partial product generation stage, where the boxed regions indicate the approximate zones in which less significant partial products are either truncated or simplified using approximate logic cells, thereby eliminating the need for exact full adder computations in those bit positions and significantly reducing the overall circuit complexity and dynamic power consumption. The horizontal dividing line separates the partial product generation stage from the partial product accumulation stage, where the lower portion of the diagram illustrates the compressed and accumulated partial product rows that are further reduced using a carry propagation network to produce the final multiplication result. The boxed groupings visible in the accumulation stage represent the approximate compressor units that combine multiple partial product bits simultaneously, replacing conventional exact carry save adder trees with simplified approximate counterparts to achieve further reductions in circuit area, propagation delay, and power dissipation. This dot diagram structure clearly demonstrates the architectural advantage of the approximate multiplier in reducing the number of active computational elements compared to a precise 8-bit multiplier, forming the foundational basis upon which the proposed NMOS power gating technique is applied to additionally suppress leakage power and achieve an overall ultra-low-power multiplication architecture suitable for energy-constrained VLSI applications.

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IV. PROPOSED METHOD

Power gated NMOS working and it's principle

NMOS power gating is an effective low-power VLSI design technique used to minimize leakage power by introducing an NMOS transistor, referred to as a "footer switch", between the logic circuit and ground (GND). This transistor functions as a controllable switch that regulates the connection of the circuit to ground based on a sleep control signal. In this configuration, the drain terminal of the NMOS footer transistor is connected to the internal logic block, while the source terminal is connected to ground. The gate terminal is driven by an external sleep signal that determines the operational state of the circuit.

During "active mode", the sleep signal is asserted HIGH, turning the NMOS transistor ON. This establishes a low-resistance path to ground, allowing the logic block to operate under normal conditions with correct voltage levels and stable switching behavior. In this state, the virtual ground node closely follows the actual ground potential, ensuring reliable circuit functionality. During "standby mode", the sleep signal is set LOW, switching the NMOS transistor OFF. This breaks the direct connection between the logic block and ground, resulting in the formation of a "virtual ground node". As a result, leakage current components such as subthreshold leakage, gate oxide leakage, and short-circuit currents are greatly reduced, leading to a significant decrease in static power consumption.

NMOS power gating is widely used in modern low-power integrated circuit design because of its simple structure, smaller area overhead, and fast switching capability.. However, the sizing of the footer transistor is a critical design consideration: an undersized transistor increases resistance and degrades performance, whereas an oversized transistor reduces leakage savings and increases silicon area utilization.

In summary, NMOS power gating offers an effective balance between power reduction and performance, making it well suited for energy-efficient applications such as embedded systems, AI accelerators, and image processing hardware.

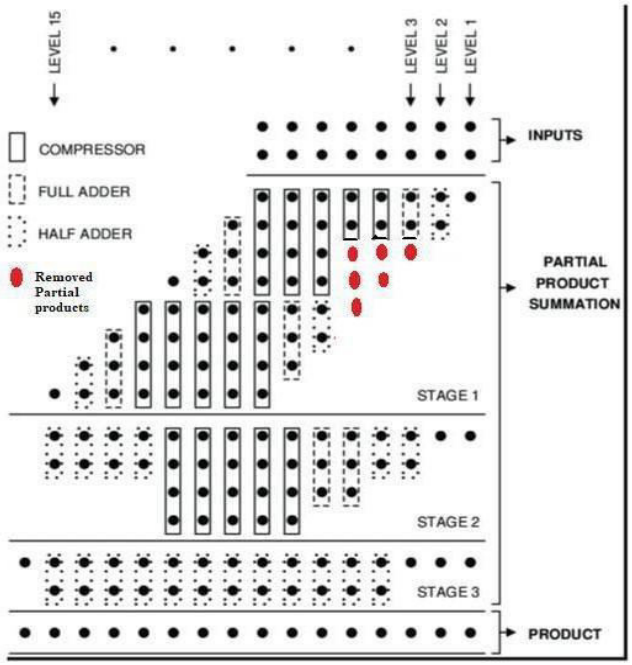

Fig. 2 . 8 bit Approximate Multiplier

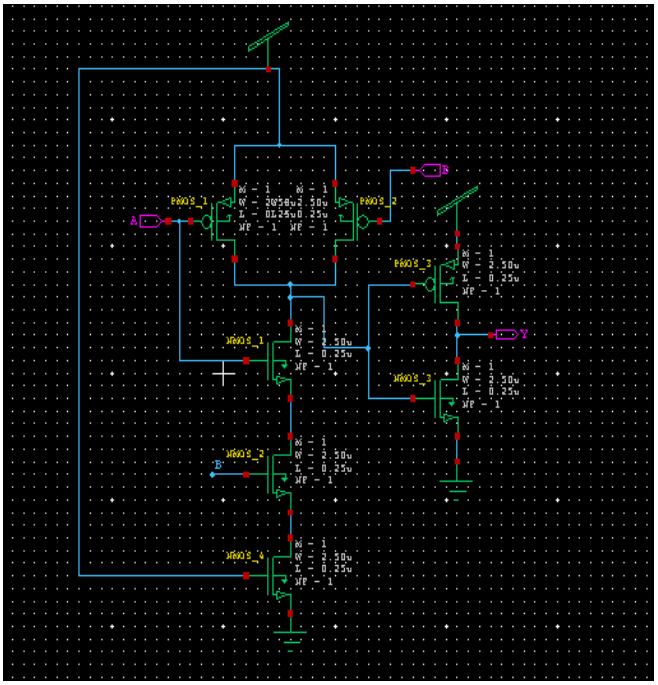

Fig.2. Power Gating NMOS Applied XOR Gate

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using Power Gating NMOS (Sleep Transistor)

In the proposed design, the NMOS power gating technique is strategically applied to the XOR gate circuit present within the half adder cells of the 8-bit approximate multiplier, wherein the XOR gate forms the most fundamental and frequently utilized logic element in the half adder structure that computes the sum output by performing exclusive OR operation between two input bits, and by inserting an NMOS sleep transistor in series with the ground terminal of the XOR gate circuit, the leakage current path is effectively cut off during the inactive or sleep mode of the multiplier operation, thereby preventing static power dissipation from occurring through the XOR gate transistors when the half adder cells are not actively participating in partial product computation.

The NMOS power gating transistor is controlled by a sleep signal such that when the sleep signal is high, the NMOS transistor turns on and connects the XOR gate circuit to the virtual ground, enabling normal active mode operation of the half adder, and when the sleep signal is de-asserted low, the NMOS transistor turns off and disconnects the XOR gate from the ground rail, effectively suppressing all leakage currents flowing through the XOR gate circuit and thereby achieving significant reduction in static power consumption compared to the conventional 8-bit approximate multiplier without power gating, with the entire proposed circuit designed and simulated using the TANNER EDA tool to validate the effectiveness of the NMOS power gating strategy in reducing overall power dissipation of the approximate multiplier architecture.

In the proposed design, the NMOS power gating technique is applied to the XOR gate circuit within the half adder cells of the 8-bit approximate multiplier, where an NMOS sleep transistor is inserted in series with the ground terminal of the XOR gate to cut off the leakage current path during inactive states. The sleep transistor is controlled by a sleep signal, enabling normal operation when active and completely suppressing leakage current when idle, thereby achieving significant reduction in static power consumption compared to the conventional 8-bit approximate multiplier implemented without power gating. The proposed circuit is designed and simulated using the Synopsys TANNER EDA tool to validate the effectiveness of the NMOS power gating strategy in reducing the overall power dissipation of the approximate multiplier architecture.

V. EXPERIMENTAL RESULT

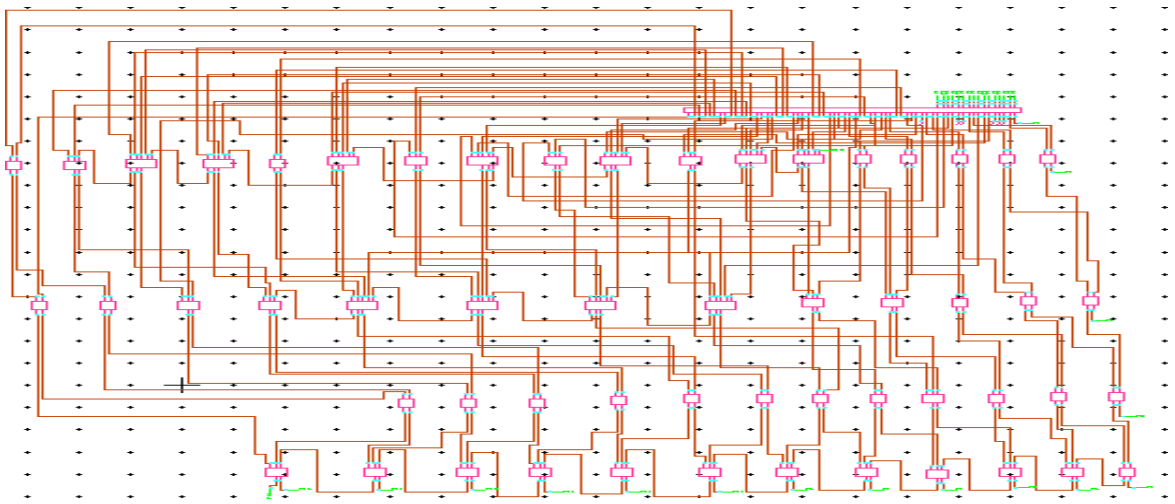

Fig. 3. Schematic of Proposed 8 Bit Multiplier

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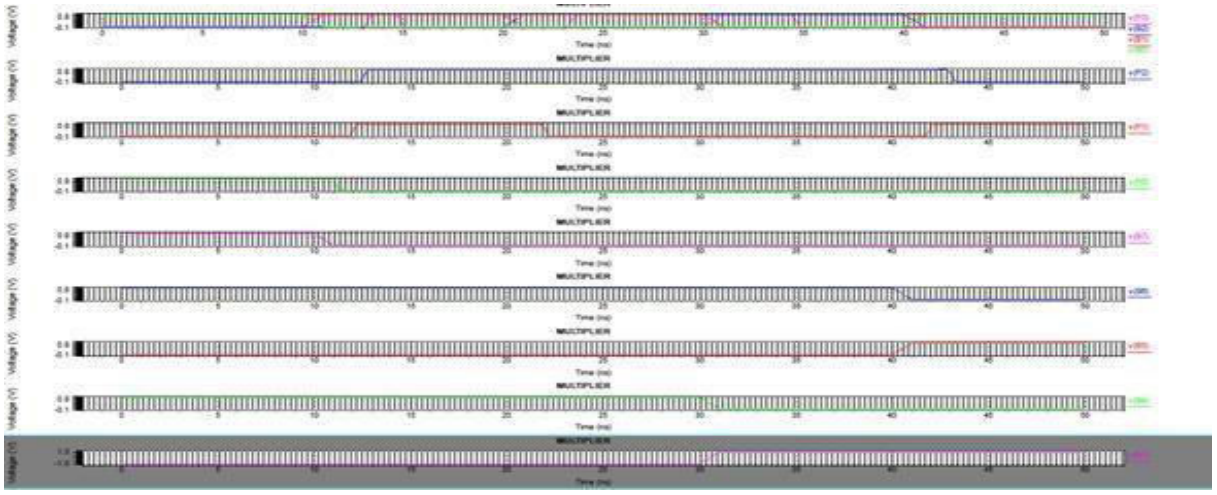

Fig. 10. Output Waveform Of Proposed 8 Bit Multiplier

The input and output waveforms of the 8-bit approximate multiplier are obtained using transient simulation in the Synopsys TANNER EDA tool. These waveforms show the time-domain behavior of two 8-bit inputs (A and B) and the corresponding 16-bit output for different input combinations. The input waveforms toggle at defined time intervals to exercise both approximate and exact computational regions of the multiplier, while the output waveforms settle to their final logic levels after the propagation delay, confirming the functional correctness of the design. The simulation further validates that the proposed NMOS power-gated approximate multiplier transitions smoothly between active and sleep modes without introducing any functional errors or glitches in the multiplication output, confirming the practical effectiveness of the proposed low-power design.

TABLE-1: COMPARISION PARAMETER TABLE

Parameter	Exact	Approximate	Approx + Power Gating
Area (µm²)	1300	1000	1100
Dynamic Power(mW)	2.8	1.8	1.8
Leakage Power (mW)	0.5	0.5	0.08
Delay (ns)	9	6	7
Power Delay Product(PDP)	29.7	13.8	13.16

TABLE-2: VOLTAGE ANALYSIS

Voltage (V)	Power (mW)	Delay (ns)
0.8	1.2	8.5
1.0	1.8	6.5
1.2	2.6	5.2

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TABLE-3: Temperature Analysis

Temperature (°C)	Power (mW)	Dela y (ns)
-120	1.1	5.0
-50	1.3	5.5
0	1.5	5.8
27	1.8	6.5
75	2.1	7.2
120	2.4	7.8

VI. RESULTS AND DISCUSSION

The simulation results obtained from the Tanner EDA tool confirm that the proposed NMOS power-gated approximate multiplier improves overall performance compared to the conventional exact design. The proposed architecture effectively reduces power consumption by lowering both dynamic and leakage components, especially during standby operation using the NMOS sleep transistor.

The delay performance is improved due to reduced computational complexity in the approximate multiplier. Although a slight delay variation is introduced with power gating because of the sleep transistor in the ground path, the overall speed remains better than the conventional design.

The area requirement is also reduced in the approximate design due to simplified partial product generation and optimized adder structures. A minor area increase is observed after introducing power gating, which is acceptable considering the significant reduction in leakage power.

The voltage and temperature analysis confirms stable circuit behavior under different operating conditions. Power and delay vary with supply voltage and temperature, but the circuit maintains correct functionality throughout.The transient response verifies proper operation of the multiplier, where all input combinations produce correct outputs and the sleep control signal successfully switches between active and standby modes without functional errors.

VII. CONCLUSION

The In this work, an approximate multiplier using NMOS-based power gating is presented to achieve reduced power consumption and improved performance. The design incorporates NMOS sleep transistors within XOR gate structures to minimize unnecessary switching activity and leakage power during inactive conditions. Approximation is mainly applied to the lower significant bit (LSB) region, while the higher significant bit (MSB) part is preserved to ensure reliable output behavior. This reduces circuit complexity and improves speed without affecting the important part of the result.

Power gating helps in lowering both dynamic and static power, which improves overall efficiency and the Power Delay Product (PDP). Therefore, the proposed design offers a simple, efficient, and scalable solution for low-power VLSI systems, making it suitable for applications like digital signal processing, image and video processing, and machine learning.

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